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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,104	10/10/2001	Warren Snyder	CYPR-CD00183	8786

7590 02/15/2006

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,104	SNYDER, WARREN	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-13 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-13 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 11/07/2005. Claims 1-2, 4-13, and 15-17 are pending in the Action.

Information Disclosure Statement

The Information Disclosure Statement filed on 11/28/2005 has been considered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4-13, and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Barnett et al, US patent no. 6,173,419 B1.

As per claim 1, Barnett anticipates an emulation method and emulator for debugging a target circuit with feature limitations very identical to the claimed invention. According to Barnett, the emulation method includes steps

Executing a sequence of instructions by a device under test, wherein the device under test comprises a data line and a clock line (col. 5, lines 7-30),

Executing the sequence of instructions by an emulator device emulating the function of the target circuit or device under test in lock-step manner with the device under test for real time debugging and improving the quality data transfer by locking input/output data for channel synchronization (Figs. 7 and 8, col. 5, lines 30-46, col. 6, line 33 to col. 7, line 10),

Conveying I/O read information from the device under test to the emulator device over the data line during a data transfer (col. 6, line 33 to col. 7, line 62),

A host computer system reading real time state and debug information from the emulator device without interrupt the device under test (cols. 5-7).

As per claim 2, Barnett anticipates the emulation in a cycle comprises data transfer and a control phase for an integration of emulation data.

As per claim 4, Barnett anticipates I/O transfer mechanism as claimed for synchronization, for instance.

As per claims 5-8 and 13, Barnett anticipates the device under test having a plurality of data lines as claimed, each claimed line could have a number of bits for information transmission as claimed (col. 6, line 51 to col. 7, line 10).

As per claims 9 and 16, Barnett anticipates an emulation method and emulator for debugging a target circuit with feature limitations very identical to the claimed invention. According to Barnett, the emulation method includes steps

Executing a sequence of instructions by a device under test, wherein the device under test comprises a data line and a clock line (col. 5, lines 7-30),

Executing the sequence of instructions by an emulator device emulating the function of the target circuit or device under test in lock-step manner with the

device under test for real time debugging and improving the quality data transfer by locking input/output data for channel synchronization (Figs. 7 and 8, col. 5, lines 30-46, col. 6, line 33 to col. 7, line 10),

Conveying I/O read information from the device under test to the emulator device over the data line during a data transfer (col. 6, line 33 to col. 7, line 62),

A host computer system reading real time state and debug information from the emulator device without interrupt the device under test (cols. 5-7), and conveying interrupt vectors or breakpoints from the microcontroller to the emulator device during an interrupt service cycle (cols. 5-7).

As per claim 10, Barnett anticipates the emulation in a cycle comprises data transfer and a control phase within the cycle for data integrity.

As per claims 11 and 12, Barnett anticipates I/O transfer mechanism such as data transfer during emulation as claimed for timing and synchronization, for instance.

As per claim 15, Barnett anticipated breakpoints of interrupt service cycles for data assertion.

As per claim 17, Barnett anticipates the device under test would include the claimed feature for emulation.

Response to Arguments

Applicant's arguments filed 11/07/2005 have been fully considered but they are not persuasive.

In response to applicant's argument Barnett does not disclose or suggest "a lockstep" as claimed, the examiner disagrees with. Barnett teaches Executing the sequence of instructions by an emulator device emulating the function of the target circuit or device under test in lock-step manner with the device under test for real time debugging and enhancing the debugging process by locking input/output sequence data and timing data for a processing synchronization and a quality of performance (Figs. 7 and 8, col. 5, lines 30-46, col. 6, line 33 to col. 7, line 10).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US patent no. 6,587,995, issued to Duboc et al, on July 2003

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Feb. 04, 2006

Thai Phan
Patent Examiner